# PHYS 235: Extra Problems (not in Lab Manual)

112. You are given a box with two terminals. You are told that the Thévenin equivalent voltage for the circuit in the box is $V_{\text{Th}} = 6\,\text{V}$ and the Thévenin equivalent resistance is $R_{\text{Th}} = 10\,\Omega$. You connect a $20\,\Omega$ resistor across the terminals of the box. Calculate the magnitude of the current that flows through the $20\,\Omega$ resistor.

113. (a) Determine the Thévenin equivalent voltage of the illustrated circuit.

(b) Determine the Thévenin equivalent resistance of the illustrated circuit. Do this two ways, and compare your results.

(c) A $100\,\Omega$ resistor is attached across the illustrated output terminals of the circuit. Determine the current through the $100\,\Omega$ resistor.
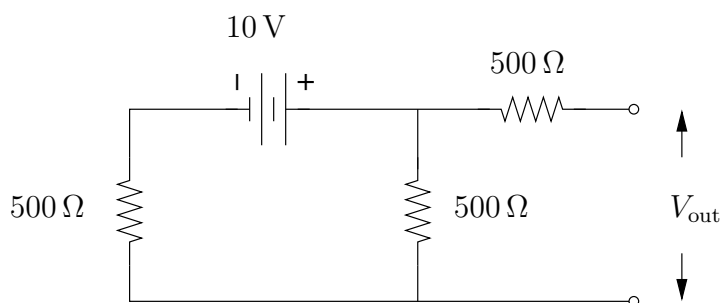

114. (a) Calculate the Thévenin equivalent voltage V_{Th} of the circuit in the shaded box. Notice the polarity of the batteries.

(b) Calculate the Thévenin equivalent resistance R_{Th} of the circuit in the shaded box. Do this two ways, and compare your results.
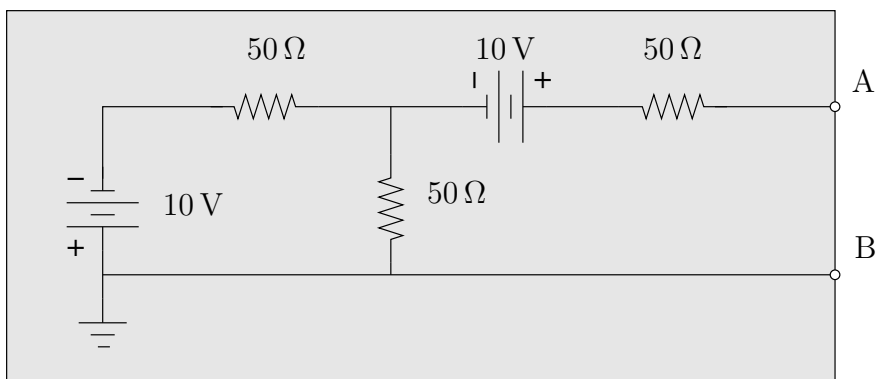
115. Consider a high-pass RC filter with a sinusoidal input v_{in} of frequency ω. Show that the amplitude of the output is
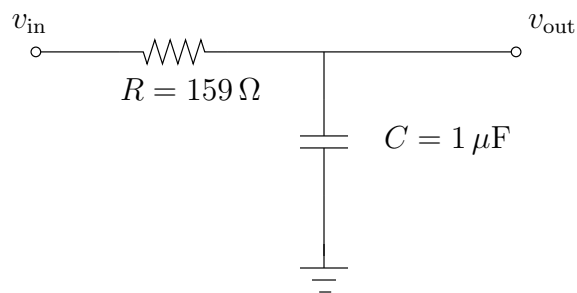
$$v_{\text{out}} = \frac{\omega RC}{\sqrt{1+(\omega RC)^2}}e^{j\tan^{-1}(1/\omega RC)}\,v_{\text{in}} = \frac{\omega RC}{\sqrt{1+(\omega RC)^2}}e^{j(\pi/2-\tan^{-1}(\omega RC))}\,v_{\text{in}}$$

116. The oscilloscope screen below shows the input voltage v_{in} for the illustrated RC circuit. You may assume that the scope is set so that the horizontal axis in the middle of the screen is ground $(0\,\text{V})$.
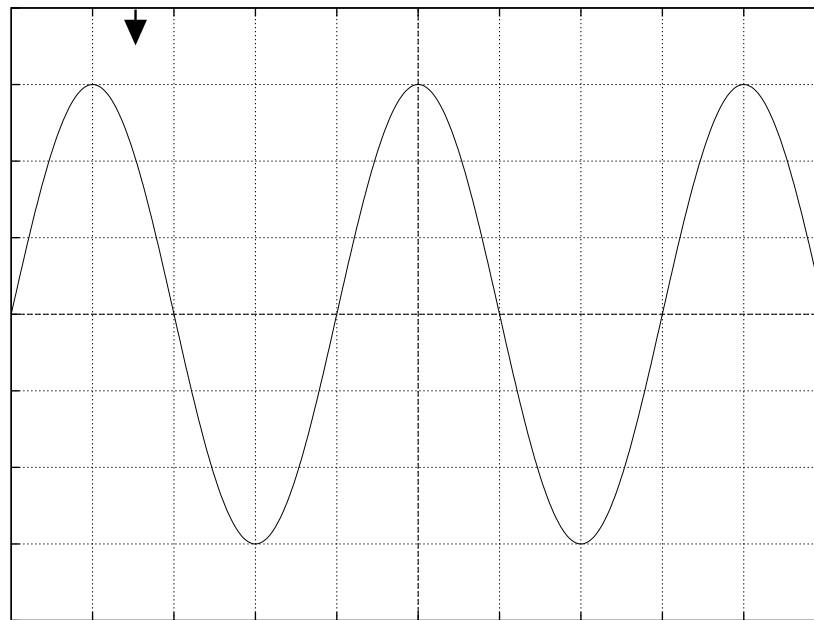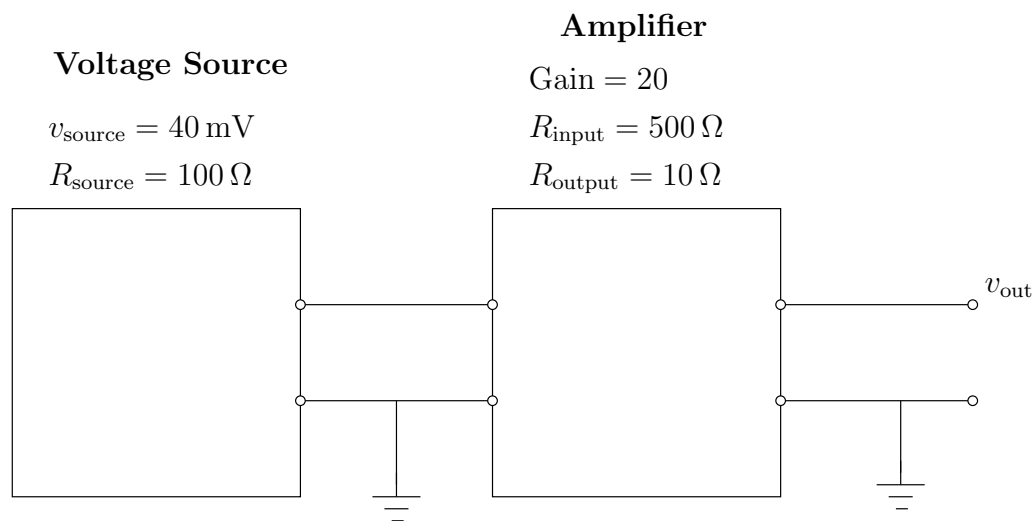

CH1 20.0 mV   250 μs

(a) What is the Trigger Slope setting: Rising or Falling?

(b) What is the Trigger Level setting?

(c) Determine the output voltage v_{out} and draw the output waveform on the graph above. (Derive all formulas you need.)

117. Determine the current flowing through the $2\,\text{k}\Omega$ resistor, the current flowing through the $3\,\text{k}\Omega$ resistor, and the current flowing through the $15\,\text{V}$ battery. **Be sure to indicate the direction of all three currents.**

$$V_A = 5\,\text{V} \qquad\qquad V_B = 15\,\text{V}$$

$$R_1 = 2\,\text{k}\Omega \qquad\qquad\qquad R_2 = 3\,\text{k}\Omega$$
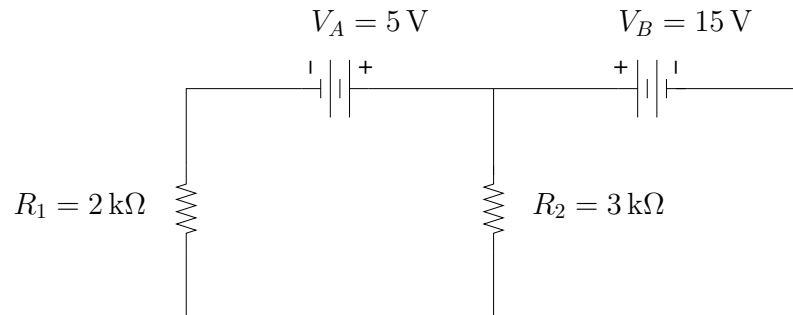
118. Consider the illustrated voltage source and amplifier. The source is set to give an output of $40\,\text{mV}$ when it has no load, and it has an output impedance of $100\,\Omega$. The amplifier voltage gain is set to 20, and the amplifier has an input impedance of $500\,\Omega$ and an output impedance of $10\,\Omega$.

   (a) Calculate the voltage at the input to the amplifier.

   (b) Calculate v_{out} when there is no load attached to the output of the amplifier.

   (c) Calculate v_{out} when a $100\,\Omega$ load resistor is attached across the output terminals of the amplifier.

Amplifier

Voltage Source

Gain $= 20$

$v_{\text{source}} = 40\,\text{mV}$

$R_{\text{input}} = 500\,\Omega$

$R_{\text{source}} = 100\,\Omega$

$R_{\text{output}} = 10\,\Omega$

v_{out}

119. Consider the illustrated circuit containing resistors and an 2N2222 NPN transistor like the transistors you used in lab. For these transistors assume that $\beta = 100$. In the first two parts of this problem you may assume the "simplest" model of transistor action, i.e., you may assume that there is no base current ($I_B = 0$). In the second two parts I want you to explore what happens if you do not make the assumption of zero base current, and use the "simple" model of transistor action in which the relationship between the base current and the collector current is $I_C = \beta I_B$, where $\beta \simeq 100$.
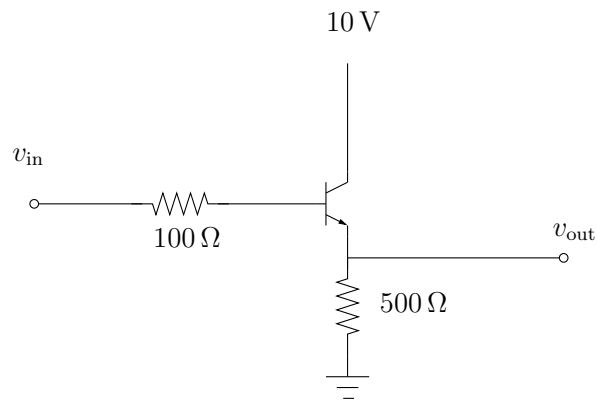

(a) Sketch the output v_{out} for the illustrated input $v_{\mathrm{in}} = 2.6\sin(2\pi \times 250t)\,\mathrm{V}$. You may assume that there is no base current for this part.
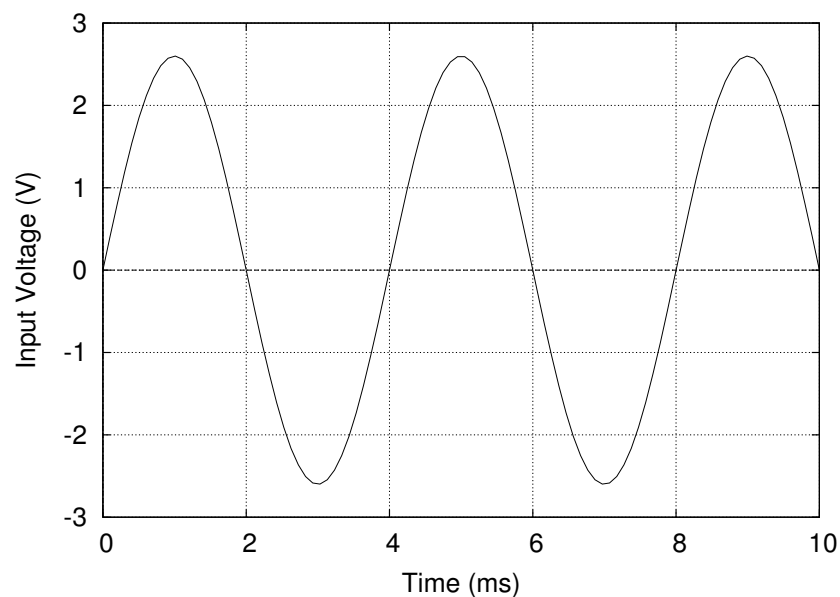
(b) Determine the peak current provided from the $10\,\mathrm{V}$ supply for the illustrated input. You may again assume that there is no base current for this part.

(c) Calculate the actual peak base current for the illustrated input using the "simple" model of transistor action. (The base current is not zero.)

(d) Calculate the peak values of I_E and I_C derived using the "simple" model.

(e) Calculate the peak base current I_B that flows if the output is accidentally connected to ground. (Use the "simple" model of transistor action.)

120. Consider the illustrated circuit containing an ideal op-amp (powered from $\pm 15\,$V supplies) and resistors. Sketch the output voltage v_{out} for the input v_{in} given in the graph. (State any assumptions you are making about the behavior of the op-amp.)

$44\,\text{k}\Omega$

v_{in}

$11\,\text{k}\Omega$

$+15$ V

-15 V
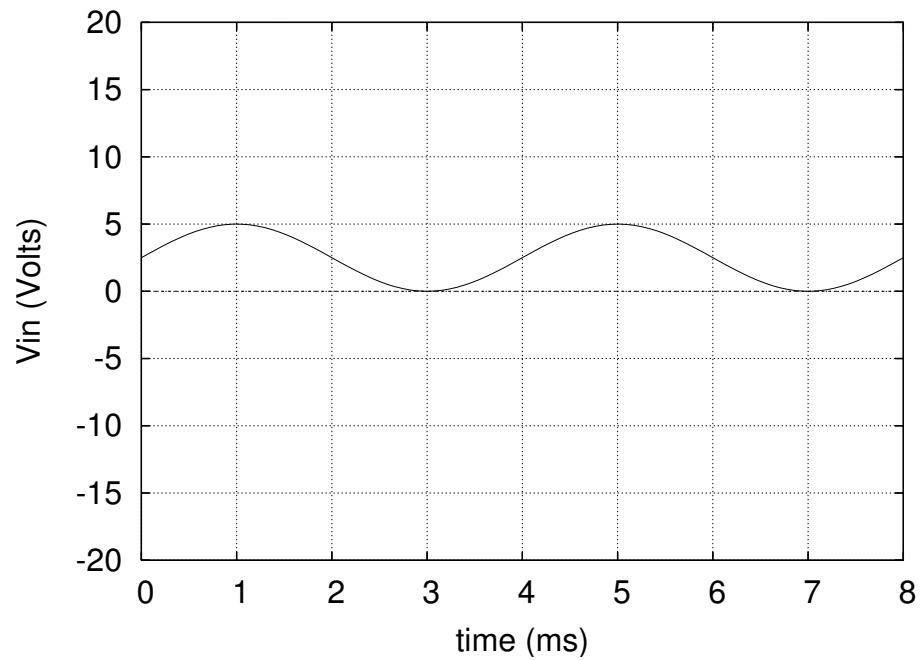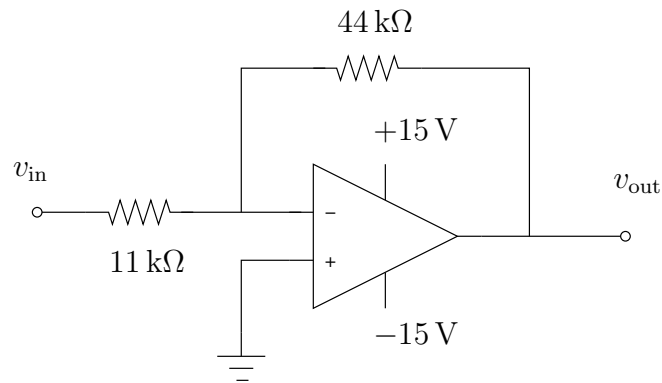
v_{out}

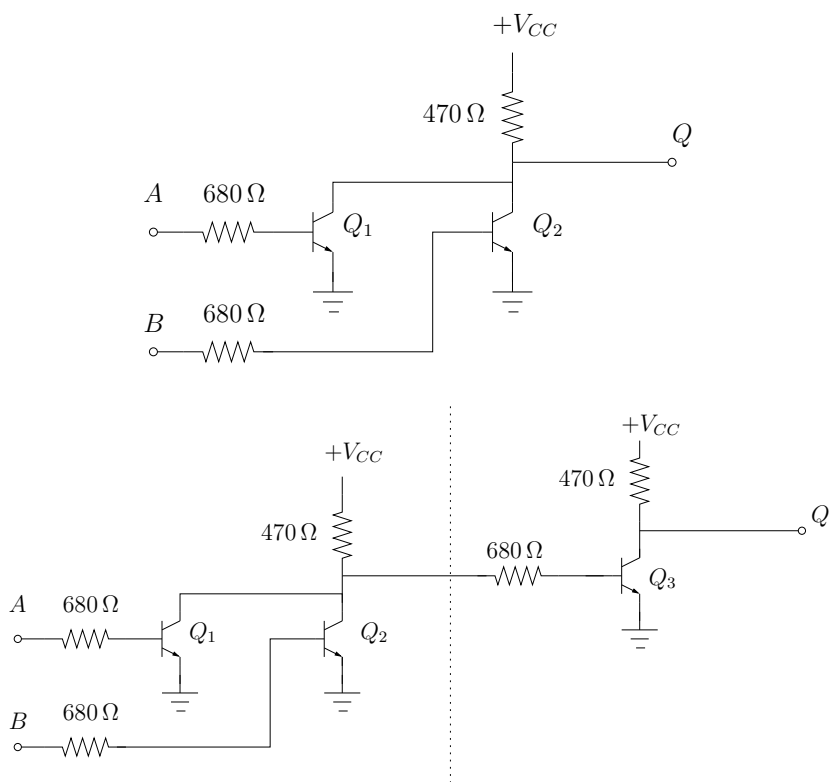121. Show that the output of the illustrated circuit is

$$v_{\text{out}} = \frac{R_2}{R_1} \left(v_B - v_A \right).$$

You may assume ideal op-amp behavior. This useful device is known as a *differential amplifier*.
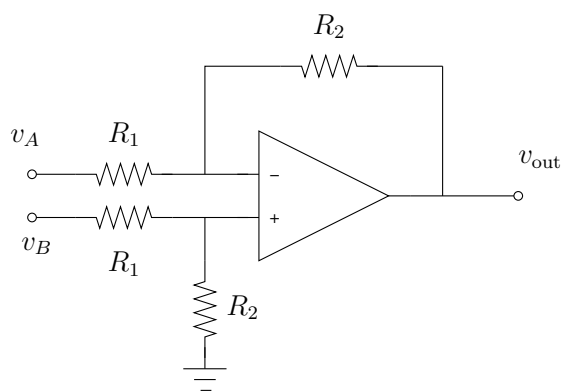

122. The illustrated circuits are realizations using transistors of two simple logic gates. What are the gates? (Explain your reasoning.)
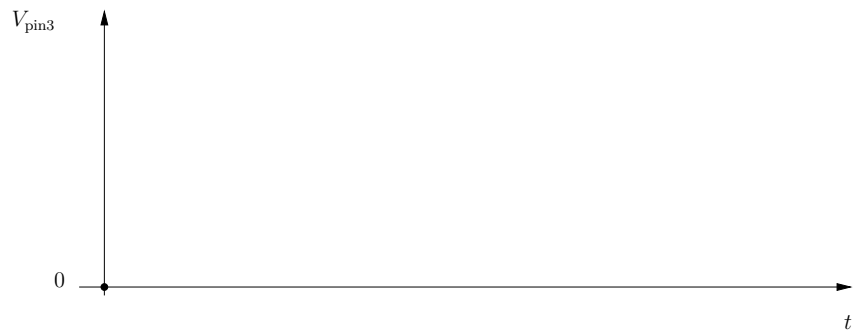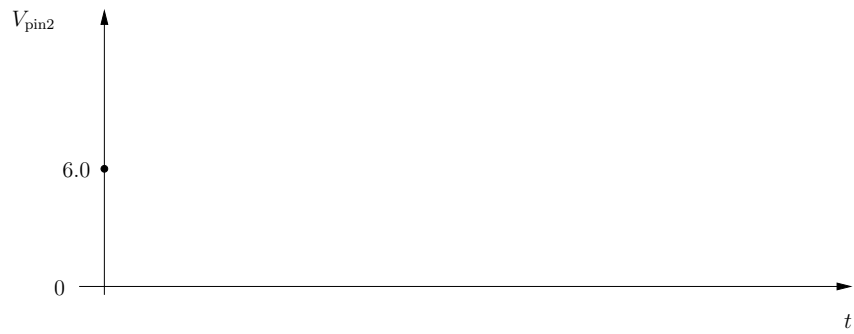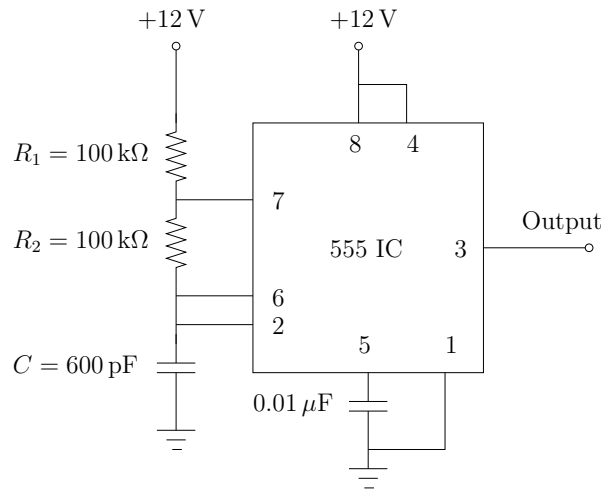
123. The illustration below is a picture of a scope face showing a voltage vs. time graph for an electrical signal. Make a sketch of what you will see if you switch to `MATH MODE` and display the `FFT` of the signal. Include labels and scales on your axes as they would appear on the scope.
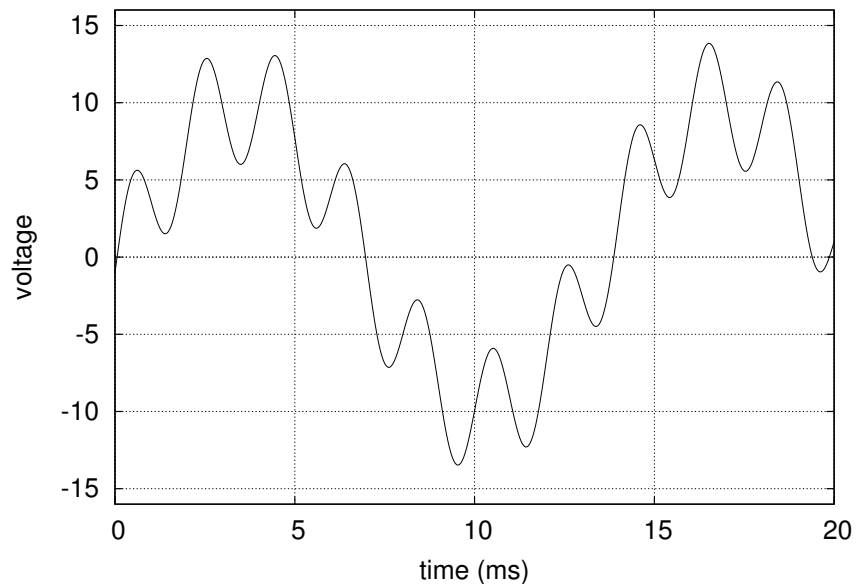
FFT
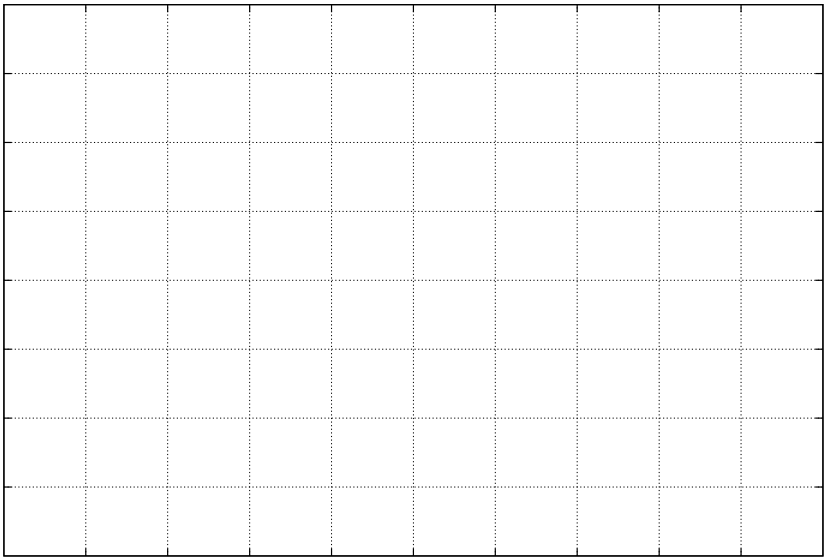
124. Sketch the indicated voltages for the illustrated circuit; include a time scale on your sketches. **NOTE:** Initial values are indicated on the graphs.

+12 V   +12 V

$R_1 = 100\,\text{k}\Omega$

8   4

7

$R_2 = 100\,\text{k}\Omega$ Output

555 IC   3

6
2

5   1

$C = 600\,\text{pF}$

$0.01\,\mu\text{F}$

V_{pin2}

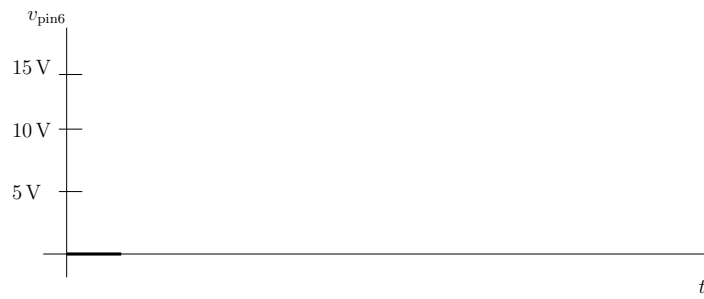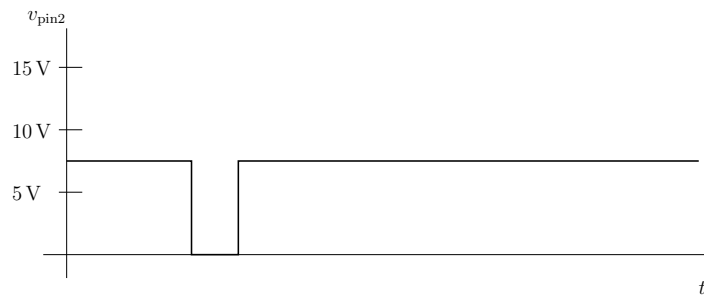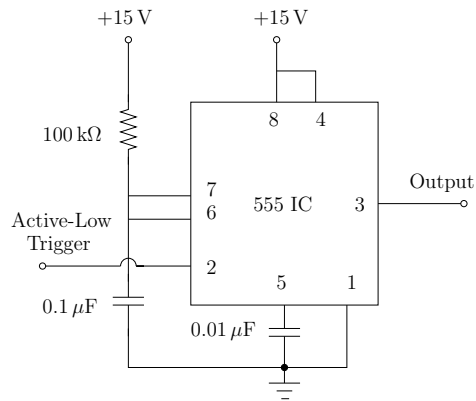6.0

0

t

V_{pin3}

0

t

125. Sketch the indicated voltages for the illustrated circuit; include a time scale on your sketches. **NOTE:** Initial values are indicated on the graphs.

+15 V   +15 V

100 kΩ

8   4

555 IC

7
6   3   Output

Active-Low
Trigger

2

5   1

0.1 μF

0.01 μF

v_{pin2}

15 V

10 V

5 V

t

v_{pin6}

15 V

10 V

5 V

t

v_{pin3}

15 V

10 V

5 V

t

126. In Lab 15 you built a cascaded decade counter circuit; see Fig. 15.1 in your lab manual. For this problem assmume that pin 4 of 4017 #1 and pin 6 of 4017 #2 are used as inputs for the first NAND gate (referred to in part 3 of the procedure) and pin 4 of 4017 #1 and pin 11 of 4017 #2 are used as inputs for the second NAND gate (referred to in part 4 of the procedure). Complete the timing diagram on the following page.

555 Clock

Pin 12 of 4017 #1

Pin 4 of 4017 #1

Pin 12 of 4017 #2

Pin 6 of 4017 #2

Output of NAND #1

Pin 5 of 4017 #1

Pin 11 of 4017 #2

Output of NAND #2

Output of Flip-Flop